What Is Claimed Is:

1. A storage control device comprising:

a first channel control section for receiving data input and output requests from a first information processing device, and transmitting and receiving data, to and from said first information processing device;

a second channel control section for receiving data input and output requests from a second information processing device, and transmitting and receiving data, to and from said second information processing device;

a disk control section for reading and writing data, from and to a storage volume storing data, in accordance with said data input and output requests; and

a cache memory for storing data transmitted and received between said first channel control section, said second channel control section and said disk control section;

wherein said first channel control section comprises:

a first memory;

a first input/output control section for receiving data input and output requests from said first information processing device and controlling transmission and reception of data between said first memory and said first information processing device;

a first processor for controlling said first memory and said cache memory; and

a first data transfer device having a first memory controller for reading and writing data from and to said first memory, and a first data transfer control section for controlling data transfer between said first memory and said cache memory;

and said second channel control section comprises:

a second memory;

a second input/output control section for controlling said second memory, receiving data input and output requests from said second information processing device and controlling transmission and reception of data between said second memory and said second information processing device;

a second processor for controlling said cache memory;

a second data transfer device having a second memory controller for reading and writing data from and to said second memory, and a second data transfer control section for controlling data transfer between said second memory and said cache memory;

and in said first channel control section;

in cases where said data input or output request received by said first input/output control section from said first information processing device is a first data write request;

said first input/output control section transmits said first data write request to said first processor;

said first processor transmits first storage position information containing information indicating a storage

position in said first memory for the first write data transmitted by said first information processing device, to said first input/output control section;

said first input/output control section starts to transmit information indicating the storage position in said first memory for said first write data, and said first write data, to said first memory controller;

said first memory controller starts to write said first write data into said first memory;

said first processor transmits first data transfer information containing information indicating the storage position in said first memory of said first write data, and information indicating a storage position in said cache memory for said first write data, to said first data transfer control section;

said first data transfer control section transmits a read request for said first write data written to said first memory, to said first memory controller, on the basis of said first data transfer information;

said first memory controller starts to read out said first write data from said first memory; and

said first data transfer control section starts to transfer said first write data read out from said first memory, to said cache memory;

and in said second channel control section;

in cases where said data input and output request received by said second input/output control section from said second information processing device is a second data write request;

said second input/output control section starts to transmit information indicating a storage position in said second memory for said second write data transmitted by said second information processing device, and said second write data, to said second memory controller;

said second memory controller starts to write said second write data into said second memory;

said second input/output control section transmits second storage position information containing information indicating the storage position in said second memory for the second write data, to said second processor;

said second processor transmits second data transfer information containing information indicating the storage position in said second memory of said second write data, and information indicating a storage position in said cache memory for said second write data, to said second data transfer control section;

said second data transfer control section transmits a read request for said second write data written to said second memory, to said second memory controller, on the basis of said second data transfer information;

said second memory controller starts to read out said second write data from said second memory; and

said second data transfer control section starts to transfer said second write data read out from said second memory, to said cache memory.

2. The storage control device according to claim 1, wherein:

in said first channel control section;

in cases where said data input or output request received by said first input/output control section from said first information processing device is a first data read request;

said first input/output control section transmits said first data read request to said first processor;

said first processor transmits third data transfer information containing information indicating the storage position in said cache memory of the first read data to be transmitted to said first information processing device, and information indicating a storage position in said first memory for said first read data, to said first data transfer control section;

said first data transfer control section starts to read out said first read data from said cache memory, on the basis of said third data transfer information;

said first data transfer control section starts to transmit information indicating the storage position in said first memory for said first read data, and said first read data, to said first memory controller;

said first memory controller starts to write said first read data into said first memory;

said first processor transmits third storage position information containing information indicating the storage position in said first memory of the first read data, to said first input/output control section;

said first input/output control section transmits a read request for said first read data written to said first memory, to said first memory controller, on the basis of said third storage position information;

said first memory controller starts to read out said first read data from said first memory; and

said first input/output control section transmits said first read data read out from said first memory to said first information processing device;

and in said second channel control section;

in cases where said data input or output request received by said second input/output control section from said second information processing device is a second data read request;

said second input/output control section transmits fourth storage position information containing information indicating a storage position in said second memory for the second read data to be transmitted to said second information processing device, to said second processor;

said second processor transmits fourth data transfer information containing information indicating the storage

position in said cache memory of said second read data, and information indicating a storage position in said second memory for said second read data, to said second data transfer control section;

said second data transfer control section starts to read out said second read data from said cache memory, on the basis of said fourth data transfer information;

said second data transfer control section starts to transmit information indicating the storage position in said second memory for said second read data, and said second read data, to said second memory controller;

said second memory controller starts to write said second read data into said second memory;

said second input/output control section transmits a read request for said second read data written to said second memory, to said second memory controller;

said second memory controller starts to read out said second read data from said second memory; and

said second input/output control section transmits said second read data read out from said second memory, to said second information processing device.

3. The storage control device according to claim 1, wherein:

in said first channel control section;

in cases where said data input or output request received by said first input/output control section from said first information processing device is a first data write request;

said first input/output control section transmits said first data write request to said first processor;

said first processor transmits said first storage position information to said first input/output control section;

said first input/output control section starts to transmit information indicating the storage position in said first memory for said first write data, and said first write data, to said first memory controller;

when transmitting said first write data, said first input/output control section appends, to each prescribed quantity of said first write data, a check code containing converted data calculated by converting said prescribed quantity of first write data in accordance with a prescribed algorithm, and error indicator data indicating whether or not there is an error in said prescribed quantity of first write data;

said first memory controller starts to write said first write data and said check code into said first memory;

said first processor transmits said first data transfer information to said first data transfer control section;

said first data transfer control section transmits a read request for said first write data and said check code written to said first memory, to said first memory controller, on the basis of said first data transfer information;

said first memory controller starts to read out said first write data and said check code from said first memory;

said first data transfer control section starts to transfer said first write data read out from said first memory, to said cache memory; and

when transferring said first write data, for each of said prescribed quantity of first write data, said first data transfer control section compares data calculated by converting said prescribed quantity of first write data in accordance with said prescribed algorithm, with said converted data in said check code appended to said prescribed quantity of first write data, and halts transfer of said first write data to said cache memory in accordance with the results of said comparison;

and in said second channel control section;

in cases where said data input and output request received by said second input/output control section from said second information processing device is a second data write request;

said second input/output control section starts to transmit information indicating the storage position in said second memory for said second write data, and said second write data, to said second memory controller;

when transmitting said second write data, said second input/output control section appends, to each prescribed quantity of said second write data, a check code containing

converted data calculated by converting said prescribed quantity of second write data in accordance with a prescribed algorithm, and error indicator data indicating whether or not there is an error in said prescribed quantity of second write data;

said second memory controller starts to write said second write data and said check code into said second memory;

said second input/output control section transmits said second storage position information to said second processor;

said second processor transmits said second data transfer information to said second data transfer control section;

said second data transfer control section transmits a read request for said second write data and said check code written to said second memory, to said second memory controller, on the basis of said second data transfer information;

said second memory controller starts to read out said second write data and said check code from said second memory;

said second data transfer control section starts to transfer said second write data read out from said second memory, to said cache memory; and

when transferring said second write data, for each of said prescribed quantity of second write data, said second data transfer control section compares data calculated by converting said prescribed quantity of second write data in accordance with said prescribed algorithm, with said converted

data in said check code appended to said prescribed quantity of second write data, and halts transfer of said second write data to said cache memory in accordance with the results of said comparison.

4. The storage control device according to claim 2, wherein:

in said first channel control section;

in cases where said data input or output request received by said first input/output control section from said first information processing device is a first data read request;

said first input/output control section transmits said first data read request to said first processor;

said first processor transmits said third data transfer information to said first data transfer control section;

said first data transfer control section starts to read out said first read data from said cache memory, on the basis of said third data transfer information;

said first data transfer control section starts to transmit information indicating the storage position in said first memory for said first read data, and said first read data, to said first memory controller;

when transmitting said first read data, said first data transfer control section appends, to each prescribed quantity of said first read data, a check code containing converted data calculated by converting said prescribed quantity of first read data in accordance with a prescribed algorithm, and

error indicator data indicating whether or not there is an error in said prescribed quantity of first read data;

said first memory controller starts to write said first read data and said check code into said first memory;

said first processor transmits said third storage position information to said first input/output control section;

said first input/output control section transmits a read request for said first read data and said check code written to said first memory, to said first memory controller, on the basis of said third storage position information;

said first memory controller starts to read out said first read data and said check code from said first memory;

each time said prescribed quantity of first read data is read out, said first data transfer control section compares data calculated by converting said prescribed quantity of first read data in accordance with said prescribed algorithm, with said converted data in said check code appended to said prescribed quantity of first read data, and writes prescribed data indicating that there is an error in said first read data, into said check code, depending on the result of this comparison;

said first input/output control section transmits said first read data read out from said first memory to said first information processing device; and

said first input/output control section halts transmission of said first read data to said first information processing device, if said prescribed data indicating that there is an error in said first read data has been written into said check code appended to each of said prescribed quantity of first read data;

and in said second channel control section;

in cases where said data input or output request received by said second input/output control section from said second information processing device is a second data read request;

said second input/output control section transmits said fourth storage position information to said second processor;

said second processor transmits said fourth data transfer information to said second data transfer control section;

said second data transfer control section starts to read out said second read data from said cache memory, on the basis of said fourth data transfer information;

said second data transfer control section starts to transmit information indicating the storage position in said second memory for said second read data, and said second read data, to said second memory controller;

when transmitting said second read data, said second data transfer control section appends, to each prescribed quantity of said second read data, a check code containing converted data calculated by converting said prescribed quantity of second read data in accordance with a prescribed algorithm,

and error indicator data indicating whether or not there is an error in said prescribed quantity of second read data;

said second memory controller starts to write said second read data and said check code into said second memory;

said second input/output control section transmits a read request for said second read data and said check code written to said second memory, to said second memory controller;

said second memory controller starts to read out said second read data and said check code from said second memory;

each time said prescribed quantity of second read data is read out, said second data transfer control section compares data calculated by converting said prescribed quantity of second read data in accordance with said prescribed algorithm, with said converted data in said check code appended to said prescribed quantity of second read data, and writes prescribed data indicating that there is an error in said second read data, into said check code, depending on the result of this comparison;

said second input/output control section transmits said second read data read out from said second memory to said second information processing device; and

said second input/output control section halts transmission of said second read data to said second information processing device, if said prescribed data indicating that there is an error in said second read data has

been written into said check code appended to each of said prescribed quantity of second read data.

5. The storage control device according to claim 1, wherein:

when said second input/output control section transmits said second storage position information to said second processor, if the writing of said second write data to said second memory has been completed;

information indicating the last write address in said second memory of said second write data, is included in said second storage position information; and

information indicating the last write address in said second memory of said second write data, is included in said second data transfer information.

6. The storage control device according to claim 1, wherein:

said first information processing device is an open information processing device; and

said second information processing device is a mainframe information processing device.

7. A storage control device comprising:

a channel control section for receiving data input and output requests from an information processing device, and transmitting and receiving data, to and from said information processing device;

a disk control section for reading and writing data, from and to a storage volume storing data, in accordance with said data input and output requests; and

a cache memory for storing data transmitted and received between said channel control section and said disk control section;

wherein said channel control section comprises:

a memory;

an input/output control section for receiving data input and output requests from said information processing device and controlling transmission and reception of data between said memory and said information processing device;

a processor for controlling said memory and said cache memory; and

a data transfer device having a memory controller for reading and writing data from and to said memory, and a plurality of data transfer control sections for controlling the transfer of data between said memory and said cache memory; wherein

in cases where said input/output control section has received a first data write request and a second data write request from said information processing device;

said input/output control section transmits said first data write request to said processor;

said input/output control section transmits said second data write request to said processor;

said processor transmits first storage position information containing information indicating a storage position in said memory for the first write data corresponding

to said first data write request transmitted by said information processing device, and second storage position information containing information indicating a storage position in said memory for the second write data corresponding to said second data write request transmitted by said information processing device, to said input/output control section;

said input/output control section starts to transmit information indicating the storage position in said memory for said first write data, and said first write data, to said memory controller;

said memory controller starts to write said first write data into said memory;

said processor transmits first data transfer information containing information indicating the storage position in said memory of said first write data, and information indicating a storage position in said cache memory for said first write data, to a first of said data transfer control sections;

said first data transfer control section transmits a read request for said first write data written to said memory, to said memory controller, on the basis of said first data transfer information;

said memory controller starts to read out said first write data from said memory;

said first data transfer control section starts to transfer said first write data read out from said memory, to said cache memory;

said input/output control section starts to transmit information indicating the storage position in said memory for said second write data, and said second write data, to said memory controller;

said memory controller starts to write said second write data into said memory;

said processor transmits second data transfer information containing information indicating the storage position in said memory of said second write data, and information indicating a storage position in said cache memory for said second write data, to a second of said data transfer control sections;

said second data transfer control section transmits a read request for said second write data written to said memory, to said memory controller, on the basis of said second data transfer information;

said memory controller starts to read out said second write data from said memory; and

said second data transfer control section starts to transfer said second write data read out from said memory, to said cache memory.

8. The storage control device according to claim 7, wherein:

in cases where said input/output control section has received said first data write request and said second data write request from said information processing device;

said input/output control section transmits said first data write request to said processor;

said input/output control section transmits said second data write request to said processor;

said processor transmits said first storage position information and said second storage position information to said input/output control section;

said input/output control section starts to transmit information indicating the storage position in said memory for said first write data, and said first write data, to said memory controller;

when transmitting said first write data, said input/output control section appends, to each prescribed quantity of said first write data, a check code containing converted data calculated by converting said prescribed quantity of first write data in accordance with a prescribed algorithm, and error indicator data indicating whether or not there is an error in said prescribed quantity of first write data;

said memory controller starts to write said first write data and said check code into said memory;

said processor transmits said first data transfer information to said first data transfer control section;

said first data transfer control section transmits a read request for said first write data and said check code written to said memory, to said memory controller, on the basis of said first data transfer information;

said memory controller starts to read said first write data and said check code from said memory;

said first data transfer control section starts to transfer said first write data read out from said memory, to said cache memory;

when transferring said first write data, for each of said prescribed quantity of first write data, said first data transfer control section compares data calculated by converting said prescribed quantity of first write data in accordance with said prescribed algorithm, with said converted data in said check code appended to said prescribed quantity of first write data, and halts transfer of said first write data to said cache memory in accordance with the results of said comparison;

said input/output control section starts to transmit information indicating the storage position in said memory for said second write data, and said second write data, to said memory controller;

when transmitting said second write data, said input/output control section appends, to each prescribed quantity of said second write data, a check code containing converted data calculated by converting said prescribed

quantity of second write data in accordance with a prescribed algorithm, and error indicator data indicating whether or not there is an error in said prescribed quantity of second write data;

said memory controller starts to write said second write data and said check code into said memory;

said processor transmits said second data transfer information to said second data transfer control section;

said second data transfer control section transmits a read request for said second write data and said check code written to said memory, to said memory controller, on the basis of said second data transfer information;

said memory controller starts to read said second write data and said check code from said memory;

said second data transfer control section starts to transfer said second write data read out from said memory, to said cache memory; and

when transferring said second write data, for each of said prescribed quantity of second write data, said second data transfer control section compares data calculated by converting said prescribed quantity of second write data in accordance with said prescribed algorithm, with said converted data in said check code appended to said prescribed quantity of write data, and halts transfer of said second write data to said cache memory in accordance with the results of said comparison.

9. A storage control device comprising:

a first channel control section for receiving data input and output requests from a first information processing device, and transmitting and receiving data, to and from said first information processing device;

a second channel control section for receiving data input and output requests from a second information processing device, and transmitting and receiving data, to and from said second information processing device;

a disk control section for reading and writing data, from and to a storage volume storing data, in accordance with said data input and output requests; and

a cache memory for storing data transmitted and received between said first channel control section, said second channel control section and said disk control section;

wherein said first channel control section comprises:

a first memory;

a first input/output control section for receiving data input and output requests from said first information processing device and controlling transmission and reception of data between said first memory and said first information processing device;

a first processor for controlling said first memory and said cache memory; and

a first data transfer device having a first memory controller for reading and writing data from and to said first

memory, and a plurality of first data transfer control sections for controlling data transfer between said first memory and said cache memory;

and said second channel control section comprises:

a second memory;

a second input/output control section for controlling said second memory, receiving data input and output requests from said second information processing device and controlling transmission and reception of data between said second memory and said second information processing device;

a second processor for controlling said cache memory; and

a second data transfer device having a second memory controller for reading and writing data from and to said second memory, and a second data transfer control section for controlling data transfer between said second memory and said cache memory;

and in said first channel control section;

in cases where said first input/output control section has received a first data write request and a second data write request from said first information processing device;

said first input/output control section transmits said first data write request to said first processor;

said first input/output control section transmits said second data write request to said first processor;

said first processor transmits first storage position information containing information indicating a storage

position in said first memory for the first write data corresponding to said first data write request transmitted by said first information processing device, and second storage position information containing information indicating a storage position in said first memory for the second write data corresponding to said second data write request transmitted by said first information processing device, to said first input/output control section;

said first input/output control section starts to transmit information indicating the storage position in said first memory for said first write data, and said first write data, to said first memory controller;

said first memory controller starts to write said first write data into said first memory;

said first processor transmits first data transfer information containing information indicating the storage position in said first memory of said first write data, and information indicating a storage position in said cache memory for said first write data, to any one of said first data transfer control sections;

said first data transfer control section, to which said first data transfer information has been transmitted, transmits a read request for said first write data written to said first memory, to said first memory controller, on the basis of said first data transfer information;

said first memory controller starts to read out said first write data from said first memory;

said first data transfer control section, to which said first data transfer information was transmitted, starts to transfer said first write data read out from said first memory, to said cache memory;

said first input/output control section starts to transmit information indicating the storage position in said first memory for said second write data, and said second write data, to said first memory controller;

said first memory controller starts to write said second write data into said first memory;

said first processor transmits second data transfer information containing information indicating the storage position in said first memory of said second write data, and information indicating a storage position in said cache memory for said second write data, to another of said first data transfer control sections which is different to said first data transfer control section to which said first data transfer information was transmitted;

said first data transfer control section, to which said second data transfer information has been transmitted, transmits a read request for said second write data written to said first memory, to said first memory controller, on the basis of said second data transfer information;

said first memory controller starts to read out said second write data from said first memory; and

said second data transfer control section, to which said first data transfer information was transmitted, starts to transfer said second write data read out from said first memory, to said cache memory; and

and in said second channel control section;

in cases where said data input and output request received by said second input/output control section from said second information processing device is a third data write request;

said second input/output control section starts to transmit information indicating a storage position in said second memory for the third write data corresponding to said third data write request transmitted by said second information processing device, and said third write data, to said second memory controller;

said second memory controller starts to write said third write data into said second memory;

said second input/output control section transmits third storage position information containing information indicating the storage position in said second memory for the third write data, to said second processor;

said second processor transmits third data transfer information containing information indicating the storage position in said second memory of said third write data, and

information indicating a storage position in said cache memory for said third write data, to said second data transfer control section;

said second data transfer control section transmits a read request for said third write data written to said second memory, to said second memory controller, on the basis of said third data transfer information;

said second memory controller starts to read out said third write data from said second memory; and

said second data transfer control section starts to transfer said third write data read out from said second memory, to said cache memory.

10. The storage control device according to claim 9, wherein:

said first information processing device is an open information processing device; and

said second information processing device is a mainframe information processing device.